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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,472	02/22/2002	Akito Yoshida	W2K 1077	4326

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EXAMINER	
ZARNEKE, DAVID A	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 05/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/082,472	YOSHIDA, AKITO	
	Examiner	Art Unit	
	David A. Zarneke	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b)

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 21-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *1-12 and 21-28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of claims 1-12 in the response dated 12/17/02 is acknowledged. The traversal is on the ground(s) that the claims are interrelated and therefore should be prosecuted together. This is not found persuasive because claims 13-20 were canceled in the response, therefore negating any claims that are restricted.

The requirement is still deemed proper and is therefore made FINAL.

Claims 21-28 were added in the above noted response. They will be examined with the presently elected claims 1-12.

Claim Rejections - 35 USC § 102(b)

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 8, 12, 22 and 28 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Otake et al., US Patent 5,805,422.

Otake teaches a semiconductor structure comprising:

a first semiconductor device (101); and

a flexible substrate means (102) coupled to a bottom surface of the first semiconductor device, wherein the flexible substrate is folded over on at least two sides

to form flap portions which are coupled to an upper surface of the first semiconductor device and covers only a portion of the upper surface of the first semiconductor device (Figures 6, 8 & 9).

Regarding claims 2, 12 and 22, Otake teaches placing an adhesive sheet (107) onto the flaps of the flexible substrate (Figure 8).

With respect to claims 8 and 28, Otake teaches a BGA device (Figures 6, 7 & 9, 10, 12 and 16).

Claims 1, 4, 5, 9, 11, 21, 24 and 25 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Fujisawa et al., US Patent 5,801,439.

Fujisawa teaches a semiconductor structure comprising:

a first semiconductor device (21); and

a flexible substrate means (24) coupled to a bottom surface of the first semiconductor device, wherein the flexible substrate is folded over on at least two sides to form flap portions which are coupled to an upper surface of the first semiconductor device and covers only a portion of the upper surface of the first semiconductor device (Figures 4, 5A-C).

Regarding claims 4 and 24, Fujisawa teaches the stacking of a 2nd device coupled to the flap portions of the substrate (Figures 9A, 9B, 10A & 10B).

With respect to claims 5 and 25, the stacking of a 2nd device coupled to the flap portions of the substrate after the flaps have been folded over onto the 1st device (Figures 9A, 9B, 10A & 10B).

As to claim 9, Fujisawa teaches a lead-type device (Figures and abstract).

Claim Rejections - 35 USC § 102(e)

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4, 5, 8, 11, 12, 21, 22, 24, 25 and 28 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Chung, US Patent 6,376,769.

Chung teaches a semiconductor stacking structure comprising:

a first semiconductor device (420); and

a flexible substrate means (410) coupled to a bottom surface of the first semiconductor device, wherein the flexible substrate is folded over on at least two sides to form flap portions which are coupled to an upper surface of the first semiconductor device and covers only a portion of the upper surface of the first semiconductor device (Figures 19 & 20).

Regarding claims 2, 12 and 22, Chung teaches placing adhesive 411-3 on the interposer that attaches the interposer to the device (Figure 19 & 21, 54+).

With respect to claims 4 and 24, Chung teaches coupling a 2nd device to the folded flap of the 1st device (Figure 21).

As to claims 5 and 25, Chung teaches attaching the 2nd device after the flaps have been folded over and coupled to the 1st device.

Regarding claims 8 and 28, Chung teaches the stacked structure to be a BGA device (30, 19+).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 7, 23 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung, US Patent 6,376,769.

Regarding claims 3 and 23, Chung fails to teach the use of an adhesive layer which is placed on the upper surface of the first semiconductor device and which couples the flap portions to the first semiconductor device.

The placement of an adhesive on the chip instead of on the interposer or in addition to being on the interposer is an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(d)).

With respect to claims 7 and 27, Chung fails to teach the specific use of this invention in a LGA, but does teach that it may be used in combination with other conventional surface mounting technology (30, 19+).

Therefore, since LGA is a conventional surface mounting technology, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the invention of Chung in a LGA device.

The use of conventional materials to perform there known functions in a conventional process is obvious. In re Raner 134 USPQ 343 (CCPA 1962).

Claims 6 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung, US Patent 6,376,769, as applied to claims 1, 11 and 21 above, and further in view of Iwase, US Patent 6,172,418, or Hashimoto et al., US Patent 6,486,544, or Kim et al., 6,225,688, or Nicewarner, Jr. et al., US Patent 5,776,797.

Chung fails to teach the 2nd device coupled to the flap portions of the flexible substrate before the flap portions are folded over and coupled to the 1st device.

Iwase, Hashimoto, Kim and Nicewarner all teach a stacked chip package wherein chips are placed on a flexible insulating film before folding into a stacked package.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the device attached to the flaps before folding of Iwase, Hashimoto, Kim and Nicewarner in the invention of Chung because these references teach that it is conventionally known in the art to formed stacked packages in this manner.

The use of conventional materials to perform there known functions in a conventional process is obvious. In re Raner 134 USPQ 343 (CCPA 1962).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chung, US Patent 6,376,769, as applied to claims 1, 11 and 21 above, and further in view of Fujisawa et al., US Patent 5,801,439.

Chung fails to teach the semiconductor stacking structure as being a lead type of device.

Fujisawa teaches a package wherein a chip is molded in an encapsulant with leads extending out of and bent around the outside the package (Figures 4 & 5A-C).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the lead-type package of Fujisawa in the invention of Chung because Chung teaches that the invention may be used in combination with other conventional surface mounting technology (30, 19+) and a lead-type package is a conventional surface mounting technology.

The use of conventional materials to perform there known functions in a conventional process is obvious. In re Raner 134 USPQ 343 (CCPA 1962).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chung, US Patent 6,376,769, as applied to claims 1, 11 and 21 above, and further in view of Otake et al., US Patent 5,805,422.

Chung fails to teach flexible substrate is folded over on four sides to form flap portions, which are coupled to the upper surface of the first semiconductor device and covers only a portion of the upper surface of the first semiconductor device.

Otake teaches a flexible circuit board having four sides that are folded over onto the attached chip (Figures 7-9 & 11).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the four-sided folds of Otake in the invention of Chung because Otake teaches that fewer fabricating steps are required (7, 55+), bending of the chip is minimized and failures of the pads at the time of installation is eliminated (7, 62+).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Isaak, US Patent 6,351,029, is cited as teaching the state of the art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (703)-305-3926. The examiner can normally be reached on M-F 10AM-6PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703)-305-9883. The fax phone numbers for the organization where this application is assigned are (703)-308-7722 for regular communications and (703)-308-7721 for After Final communications.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703)-308-0956.

David A. Zarneke
May 2, 2003